IN THE CLAIMS:

Amend claims 1, 2, 5, 6, 8, 9, 12, 13, 16, 17 and add new claims 18-23 as shown in the following listing of claims, which replaces all previous versions and listings of claims in this application.

1. (currently amended) A memory interface device ~~to control a~~ for controlling memory access ~~with respect to: a~~ between a memory write unit that writes data into a memory and a memory readout unit that reads the data from the memory, the memory write unit being in compliance ~~to comply~~ with a memory write procedure in which ~~every~~ each time data is written into a memory ~~every~~ by a predetermined ~~amount~~ unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is ~~performed; and a memory readout unit which reads the data from the memory~~ performed, the memory interface device comprising:

write detection means for detecting the write of the predetermined ~~amount~~ unit amount of the data ~~from~~ by the memory write unit into the memory;

signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the write detection means, a signal to notify the memory write unit that the readout of the data from the memory by the memory

readout unit has been ~~completed, in a case where~~ completed; ~~the write of the predetermined amount unit of the data is detected;~~

data storage amount measurement means for measuring an amount of the data stored in the memory during the memory write procedures; ~~and~~

memory readout control means for generating an interrupt signal with respect to the memory readout ~~unit, in a case where~~ unit when the stored data amount in the memory reaches a predetermined readout start storage ~~amount.~~ amount; and

a timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout signal to the memory readout control means when a value of the period count reaches a predetermined timer period, the memory readout control means generating the interrupt signal with respect to the memory readout unit even when the memory readout control means receives the timeout signal output from the timer.

2. (currently amended) A memory interface device ~~connected~~ for connection to a memory write unit ~~to comply~~ to control a memory access to the memory write unit, the memory write unit being in compliance with a memory write procedure in which ~~every~~ each time data is written into a memory by a ~~every~~ predetermined ~~amount~~ unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is ~~performed;~~

~~the memory interface device being configured to control a memory access to the memory write unit, the~~ performed, the memory interface device comprising:

write detection means for detecting the write of the predetermined ~~amount~~ unit amount of the data ~~from~~ by the memory write unit into the memory;

signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the write detection means, a signal to notify the memory write unit that ~~the~~ readout of the data from the memory has been ~~completed, in a case where the write of the predetermined amount unit of the data is detected~~ completed;

data storage amount measurement means for measuring an amount of the data stored in the memory during the memory write procedures;

data processing means for reading the data from the memory ~~to subject~~ and for subjecting the read data to predetermined processing; ~~and~~

memory readout control means for generating an interrupt signal with respect to the data processing ~~means, in a case where~~ means when the stored data amount in the memory reaches a predetermined readout start storage ~~amount.~~ amount; and

a timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout

signal to the memory readout control means when a value of the period count reaches a predetermined timer period, the memory readout control means generating the interrupt signal with respect to the data processing means even when the memory readout control means receives the timeout signal output from the timer.

3.-4. (canceled)

5. (currently amended) A memory interface method ~~to control a~~ for controlling memory access ~~with respect to: a~~ between a memory write unit that writes data into a memory and a memory readout unit that reads the data from the memory, the memory write unit being in compliance ~~to comply~~ with a memory write procedure in which ~~every~~ each time data is written into a memory ~~every~~ by a predetermined ~~amount~~ unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is ~~performed; and a memory readout unit which reads the data from the memory, the~~ performed, the memory interface method comprising:

a step of detecting the write of the predetermined ~~amount~~ unit amount of the data ~~from~~ by the memory write unit into the memory;

a step of notifying the memory write unit, upon detection of the writing of the predetermined unit amount of the data, that the readout of the data from the memory by the memory

readout unit has been ~~completed, in a case where the write of the predetermined amount unit of the data is detected~~ completed;

a step of measuring an amount of the data stored in the memory during the memory write procedures; ~~and~~

a step of generating an interrupt signal with respect to the memory readout ~~unit, in a case where~~ unit when the stored data amount in the memory reaches a predetermined readout start storage ~~amount.~~ amount;

a step of counting a period in which writing of the predetermined unit amount of the data is discontinued; and

a step of generating the interrupt signal with respect to the memory readout unit when a value of the period count reaches a predetermined timer period.

6. (currently amended) ~~The~~ A memory interface method according to claim ~~5, further comprising: a~~ 5; further comprising a step of temporarily stopping notification to the memory write unit that the readout of the data from the memory has been completed when ~~the readout completion notice, in a case where~~ the stored data amount in the memory reaches the predetermined readout start storage amount.

7. (canceled)

8. (currently amended) A memory interface device for controlling ~~to control a~~ memory access between a ~~with respect to: a~~ first memory write and readout unit and a second memory write

and readout unit which write and read data with respect to a memory, the first memory write and readout unit being in compliance ~~to comply~~ with a memory write procedure in which ~~every~~ each time data is written into a memory ~~every~~ by a predetermined ~~amount~~ unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is ~~performed; and a second memory write and readout unit which writes and reads the data with respect to the memory, the~~ performed, the memory interface device comprising:

first write detection means for detecting the write of the predetermined ~~amount~~ unit amount of the data ~~from~~ by the first memory write and readout unit into the memory;

first completion signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the first write detection means, a completion signal to notify the first memory write and readout unit that the readout of the data from the memory has been ~~completed, in a case where the write of the predetermined amount unit of the data is detected~~ completed;

first data storage amount measurement means for measuring an amount of the data stored in the memory during the memory write procedures;

first memory readout control means for generating an interrupt signal with respect to the second memory write and

readout ~~unit, in a case where~~ unit when the stored data amount in the memory reaches a predetermined readout start storage amount;

second write ~~amount~~ detection means for detecting the write of the predetermined amount of the data from the second memory write and readout unit into the memory;

second completion signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the second write detection means, a completion signal to notify the first memory write and readout unit that the write of the data into the memory has been ~~completed, in a case where the write of the predetermined amount of the data is detected~~ completed;

second data storage amount measurement means for measurement the stored data amount in the memory during the memory write procedures; ~~and~~

second memory readout control means for generating an interrupt signal with respect to the second memory write and readout ~~unit, in a case where~~ unit when the stored data amount in the memory reaches a predetermined readout completion storage ~~amount.~~ amount; and

a first timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout signal to the first memory readout control means when a value of the period count reaches a predetermined timer period, the first

memory readout control means generating the interrupt signal with respect to the second memory write and readout unit even when the first memory readout control means receives the timeout signal output from the first timer.

9. (currently amended) ~~The~~ A memory interface device according to claim ~~8, wherein~~ 8; wherein the first memory readout control means temporarily stops the signal generation by the first completion signal generation ~~means, in a case where~~ means when the stored data amount in the memory reaches the predetermined readout start storage amount.

10.-11. (canceled)

12. (currently amended) A memory interface method for controlling ~~to control a~~ memory access between a ~~with respect to: a~~ first memory write and readout unit and a second memory write and readout unit which write and read data with respect to a memory, the first memory write and readout unit being in compliance ~~to comply~~ with a memory write procedure in which ~~every~~ each time data is written into a memory ~~every~~ by a predetermined ~~amount~~ unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is ~~performed; and a second memory write and readout unit which writes and reads the data with respect to the memory, the~~ performed, the memory interface method ~~including~~ comprising:

a step of detecting the write of the predetermined ~~amount~~ unit amount of the data from the first memory write and readout unit into the memory;

a step of notifying the first memory write and readout unit, upon detection of the predetermined unit amount of the data, that the readout of the data from the memory has been ~~completed, in a case where the write of the predetermined amount unit of the data is detected~~ completed;

a step of measuring an amount of the data stored in the memory as a result of the memory write procedures;

a step of generating an interrupt signal with respect to the second memory write and readout ~~unit, in a case where~~ unit when the stored data amount in the memory reaches a predetermined readout start storage amount;

a step of detecting the write of the predetermined amount of the data from the second memory write and readout unit into the memory;

a step of generating a signal, upon detection of the writing of the predetermined amount of data, to notify the first memory write and readout unit that the write of the data into the memory has been ~~completed, in a case where the write of the predetermined amount of the data is detected~~ completed;

a step of measuring the stored data amount in the memory; ~~and~~

a step of generating an interrupt signal with respect to the second memory write and readout ~~unit, in a case where~~ unit when the stored data amount in the memory reaches a predetermined readout completion storage ~~amount.~~ amount;

a step of counting a period in which the write of the predetermined unit amount of the data is discontinued; and

a step of generating the interrupt signal with respect to the second memory write and readout unit when the a value of the period count reaches a predetermined timer period.

13. (currently amended) ~~The~~ A memory interface method according to claim ~~12, further comprising a~~ 12; further comprising a step of temporarily stopping the readout completion ~~notice, in a case where~~ notice when the stored data amount in the memory reaches the predetermined readout start storage amount.

14.-15. (canceled)

16. (currently amended) A modem device ~~connected~~ for connection to a data processing unit ~~to comply~~ that complies with a memory write procedure in which ~~every~~ each time communication data or control command data is written into a memory ~~every~~ by a predetermined ~~amount~~ unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next write of the data into the memory is performed, the modem device comprising:

~~the modem device comprising: a~~ a modem interface ~~which~~ that exchanges ~~the~~ communication data or control command data with respect to the data processing unit; ~~the memory; a memory readout unit which reads the data from the memory; and communication means connected to the memory readout unit to transmit and receive the communication data,~~

a memory into which the communication data or control command data is written;

a memory readout unit that reads the communication data or control command data from the memory;

communication means connected to the memory readout unit to transmit and receive the communication data or the control command data;

~~the modem device further comprising:~~

write detection means for detecting the write of the predetermined ~~amount~~ unit amount of the communication data or the control command data from the ~~memory write~~ data processing unit into the memory;

signal generation means for generating, upon detection of the writing of the predetermined unit amount of the communication data or the control command data, a signal to notify the data processing unit that the readout of the communication data or the control command data from the memory has been ~~completed, in a case where the write of the predetermined amount unit of the data is detected~~ completed;

data storage amount measurement means for measuring an amount of the communication data or the control command data stored in the memory; ~~and~~

memory readout control means for generating an interrupt signal with respect to the memory readout ~~unit, in a case where~~ unit when the stored data amount in the memory reaches a predetermined readout start storage ~~amount.~~ amount; and

counting means for counting a period in which writing of the predetermined unit amount of the data into the memory is discontinued and for outputting a timeout signal to the memory readout control means when a predetermined value of the period count is reached, the memory readout control means generating the interrupt signal with respect to the memory readout unit even when the memory readout control means receives the timeout signal.

17. (currently amended) A modem device ~~connected~~ for connection to a data processing unit ~~to comply~~ that complies with a memory write procedure in which ~~every~~ each time communication data or control command data is written into a memory ~~every~~ by a predetermined ~~amount~~ unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next write of the data into the memory is performed, the modem device comprising:

~~the modem device comprising: a~~ a modem interface ~~which~~ that exchanges ~~the~~ communication data or control command data

with respect to the data processing ~~unit; the memory; a memory write and readout unit which writes and reads the data with respect to the memory; and communication means connected to the memory write and readout unit to transmit and receive the communication data,~~ unit;

~~the modem device further comprising:~~

a memory into which the communication data or control command data is written;

a memory write and readout unit that writes and reads the communication data or control command data from the memory;

communication means connected to the memory write and readout unit to transmit and receive the communication data or the control command data;

write detection means for detecting the write of the predetermined ~~amount~~ unit amount of the communication data or the control command data from the memory write and readout unit into the memory;

first completion signal generation means for generating, upon detection of the writing of the predetermined unit amount of the communication data or the control command data, a signal to notify the data processing unit that the readout of the communication data or the control command data from the memory has been ~~completed, in a case where the write of the predetermined amount unit of the data is detected~~ completed;

first data storage amount measurement means for measuring an amount of the data stored in the memory; ~~first memory readout control means for generating an interrupt signal with respect to the memory write and readout unit, in a case where the stored data amount in the memory reaches a predetermined readout start storage amount;~~

first memory readout control means for generating an interrupt signal with respect to the memory write and readout unit when the stored data amount in the memory reaches a predetermined readout start storage amount;

write amount detection means for detecting the write of the predetermined amount of the data from the memory write and readout unit into the memory;

second completion signal generation means for generating, upon detection of the writing of the predetermined amount of the data, a signal to notify the data processing unit that the write of the data into the memory has been ~~completed, in a case where the write of the predetermined amount of the data is detected~~ completed;

second data storage amount measurement means for measurement the stored data amount in the memory; ~~and~~

second memory readout control means for generating an interrupt signal with respect to a second memory write and readout ~~unit, in a case where~~ unit when the stored data amount in

the memory reaches a predetermined readout completion storage ~~amount.~~ amount; and

counting means for counting a period in which writing of the predetermined unit amount of the data into the memory is discontinued and for outputting a timeout signal to the first memory readout control means when a predetermined value of the period count is reached, the first memory readout control means generating the interrupt signal with respect to the memory write and readout unit even when the first memory readout control means receives the timeout signal.

18. (new) A memory interface device according to claim 1; wherein the memory readout control means temporarily stops the signal generation by the signal generation means when the stored data amount in the memory reaches the predetermined readout start storage amount.

19. (new) A memory interface device according to claim 2; wherein the memory readout control means temporarily stops the signal generation by the signal generation means when the stored data amount in the memory reaches the predetermined readout start storage amount.

20. (new) A memory interface device according to claim 8; further comprising a second timer that counts a period in which the write of the data from the second memory write and readout unit into the memory is discontinued when a value of the

period count reaches a predetermined timer period, the second timer outputting a timeout signal to the second completion signal generation means; and wherein the second completion signal generation means generates a completion notice signal with respect to the first memory write and readout unit upon receipt of the timeout signal.

21. (new) A memory interface device according to claim 9; further comprising a second timer that counts a period in which the write of the data from the second memory write and readout unit into the memory is discontinued when a value of the period count reaches a predetermined timer period, the second timer outputting a timeout signal to the second completion signal generation means; and wherein the second completion signal generation means generates a completion notice signal with respect to the first memory write and readout unit upon receipt of the timeout signal.

22. (new) A memory interface method according to claim 12; further comprising: a step of counting a period in which the write of the data from the second memory write and readout unit into the memory is discontinued; a step of outputting a timeout signal when a value of the period count reaches the predetermined timer period; and a step of outputting a completion signal to the first memory write and readout unit in response to the timeout signal.

23. (new) A memory interface method according to claim 13; further comprising: a step of counting a period in which the write of the data from the second memory write and readout unit into the memory is discontinued; a step of outputting a timeout signal when a value of the period count reaches the predetermined timer period; and a step of outputting a completion signal to the first memory write and readout unit in response to the timeout signal.